REMARKS

The Examiner's Final Office Action of December 26, 2002 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application, and for indicating that claims 3 and 5 as containing allowable subject matter.

Claims 1-11 were pending in the present application, of which claim 1 is independent. By the above actions, claims 1, 8, and 9 have been amended, and new claims 12-16 have been added. Accordingly claims 1-16 are pending, of which claims 1 and 15 are independent. In view of these actions and the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, the drawings are objected to under 37 CFR 1.83(a), stating the drawings must show every feature of the invention specified in the claims. The Examiner states that the limitations "an upper interlevel dielectric film formed to cover the first interconnection layer; a second interconnection layer formed on the upper interlevel dielectric film" in claim 9 must be shown or the features cancelled from the claim. Further, claim 8 is rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The Examiner asserts that the phrase "a second interval dielectric film formed to cover the first interconnection layer" is not described in the specification and not shown in the figures.

In response to the drawing objection and the §112, first paragraph, rejection, Applicants have amended claim 9, as well as claim 8, as shown, above to change "a second interlevel dielectric film" to "an upper interlevel dielectric film".

Specifically, with respect to amended claim 8, the feature of "An upper interlevel dielectric film formed to cover the first interconnection layer" in the amended claim 8 corresponds with "a third interlevel dielectric film formed over the storage lines 20" in page 12, lines 22-24 of the present specification. Hence, the amendment of claim 8 is supported by the present specification. Further, the amended claim 8 is also supported by the drawings.

In contrast with amended claim 8, the feature of "a first interlevel dielectric film" in the amended claim 1 corresponds to "a second interlevel dielectric film" in the present

specification.

With respect amended claim 9, to facilitate the explanation of the present invention, Applicants are submitting herewith drawings of the upper interlevel dielectric film and the second interconnection layer disclosed in Figs. 1, 2, and 4 and denoted by hand-written notes. Support for the description shown in the attached drawings can be found at least in, e.g., page 12, lines 22-24 of the present specification.

Claims 1, 2, 4, 6-8 and 11 stand rejected under 35 U.S.C. §103(a) as unpatentable over Applicant Admitted Prior Art (Figs. 4-5 and pages 2-3) in view of Chinu et al. (JP 11121705A – hereafter Chinu) previously applied. Further, claims 9-10 stand rejected under 35 U.S.C. §103(a) as unpatentable over Chinu in view of Hayashi et al. (U.S. Patent No. 6,174,766 B1 – hereafter Hayashi).

According to the present invention, as shown in attached Fig. 1, the storage line (i.e., first interconnection layer) 20 connected to the top electrode (TE) and the diffusion layer of the transistor via the contact (CW1) extends in a Y direction, which is orthogonal to the extending X direction of the bottom electrode (CPO). In the Y direction, the storage line (first interconnection layer) 20 is formed such that it only extends over the ends of the top (TE) and bottom (CPO) electrodes on the same side, such as denoted by ↓ in the attached Fig. 1. In other words, the storage line (first interconnection layer) 20 is not formed over the ends of the top (TE) and bottom (CPO) electrodes in the direction opposite to the Y direction, and the top and bottom electrodes are in a free state.

Hence, a stress applied by the storage line (first interconnection layer) 20 to the ferroelectric capacitor or a leakage current flowing between adjacent portions of the storage line (first interconnection layer) 20 is decreased, thus preventing a decrease in early yield resulting from leakage failure and deterioration in retention characteristics. As a result, the reliability of the ferroelectric memory device can be improved.

In contrast with the present invention, the prior art (i.e., APA), as shown in Figs. 4-5, shows the storage line (first interconnection layer) 20 connected to the top electrode (TE) and the diffusion layer of the transistor via the contact (CW1) extends in a direction (Y direction) orthogonal to the extending direction (X direction) of the bottom electrode (CPO). However, in the Y direction, the storage line (first interconnection layer) 20 is formed such that it extends over <u>both</u> ends of the top (TE) and bottom (CPO) electrodes, as denoted by the hand-

marking ↑ and ↓ in the attached Fig. 4. In other words, the storage line (first interconnection layer) 20 is also formed over the ends of the top (TE) and bottom (CPO) electrodes in the direction opposite to the Y direction. Thus, stress applied to the ferroelectric capacitor or a leakage current of the storage line (first interconnection layer) 20 increases.

With respect to Chinu, as disclosed in Figs. 4-7, the storage line (first interconnection layer) 73 connected to the top electrode 67a and the diffusion layers of the transistor 57a, 57b extends in a direction (X direction) orthogonal to the extending direction (Y direction) of the bottom electrode 63a. However in the X direction, the storage line (first interconnection layer) 73 exists on both the left and right sides.

To illustrate and compare the disclosed invention of Chinu and the presently claimed invention, Applicants is submitting herewith the attached Fig. 6 illustrating the device of Chinu. As shown in the attached Fig. 6, the storage line 73 is formed such that it extends over both ends of the bottom electrode 63a in the X direction, which is denoted by the hand-drawn arrows ← and → shown therein. Accordingly, the storage line (first interconnection layer) 73 also extends over the bottom electrode 63a of the ferroelectric capacitor, and thus stress applied to the ferroelectric capacitor or a leakage current of the first interconnection layer increases.

As presented above, APA and Chinu fails to teach, disclose, or suggest Applicants invention as recited in the amended independent claims 1 and dependent claim 8 and 9, as well as the remaining pending dependent claims.

Moreover, in the APA and Chinu, stress applied to the ferroelectric capacitor or a leakage current of the first interconnection layer increases, while in the presently claimed invention stress applied to the ferroelectric capacitor or a leakage current of the first interconnection layer decreases. Hence, the presently claimed invention is distinguishable over the APA and Chinu.

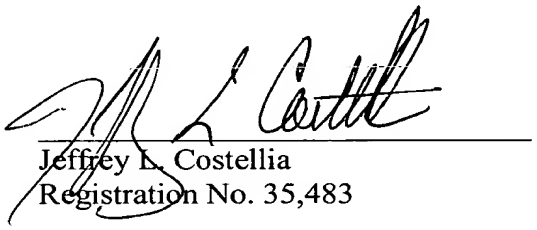
In view of the amendments and arguments set forth above, Applicants respectfully requests reconsideration and withdrawal of all the drawing objection, and pending §112 and 103(a) rejections.

New claims 12-16 have been added to further complete the scope to which Applicants are entitled. New claim 12 includes the features of claim 1-3 prior to the amendment of claim 1 above. New claim 13, which depends from claim 12, includes the features of claim 4. New

claim 14, which depends from claim 13, includes the features of claim 5. New claim 16, which depends from claim 15, includes the features of claim 7.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,



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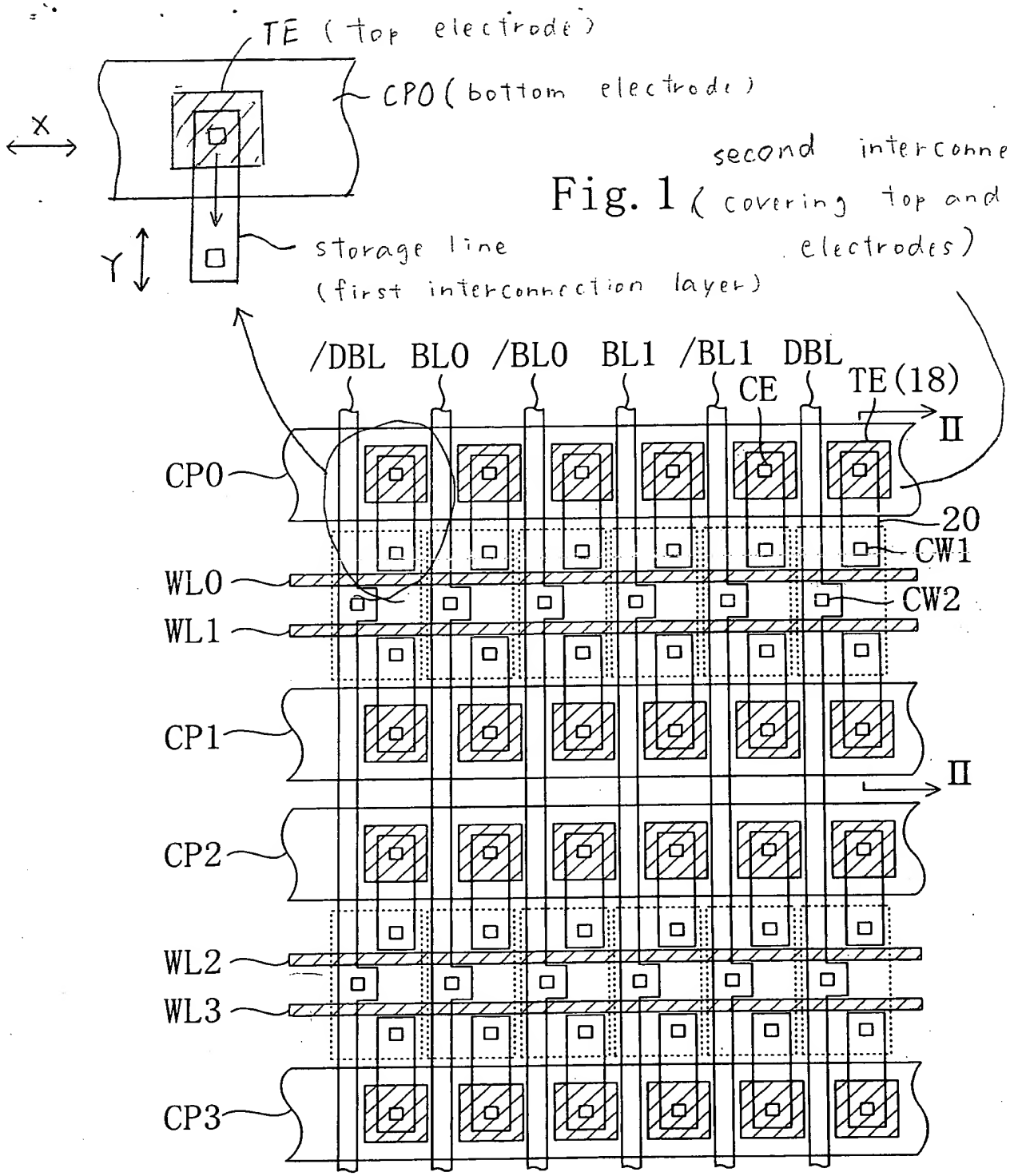


Fig. 1

ATTACHMENT
FIG. 1 OF THE PRESENT INVENTION

Amendment

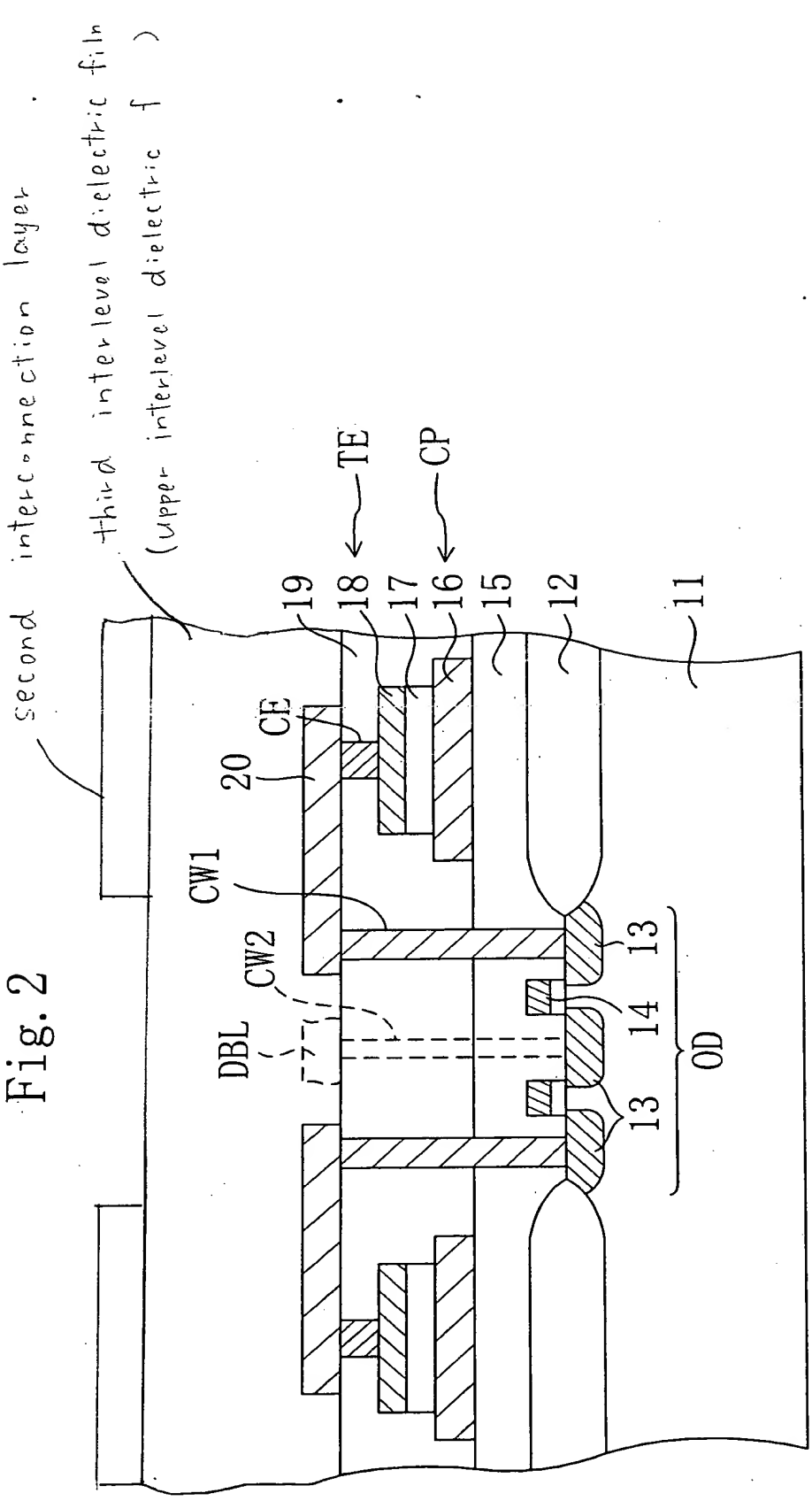


Fig. 2

ATTACHMENT
FIG. 2 OF THE PRESENT INVENTION

Reference

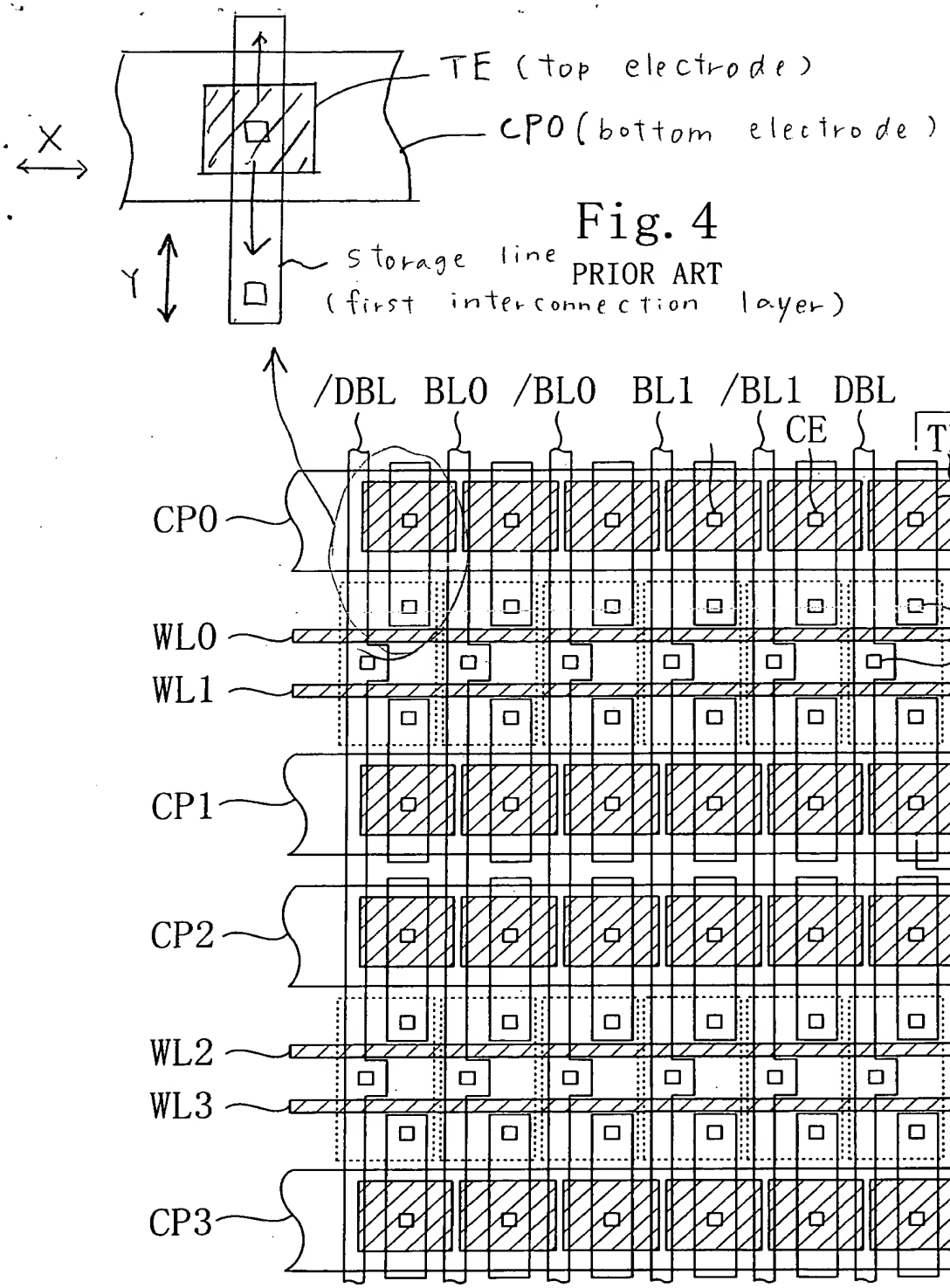


Fig. 4
PRIOR ART

ATTACHMENT
FIG. 4 PRIOR ART

Reference

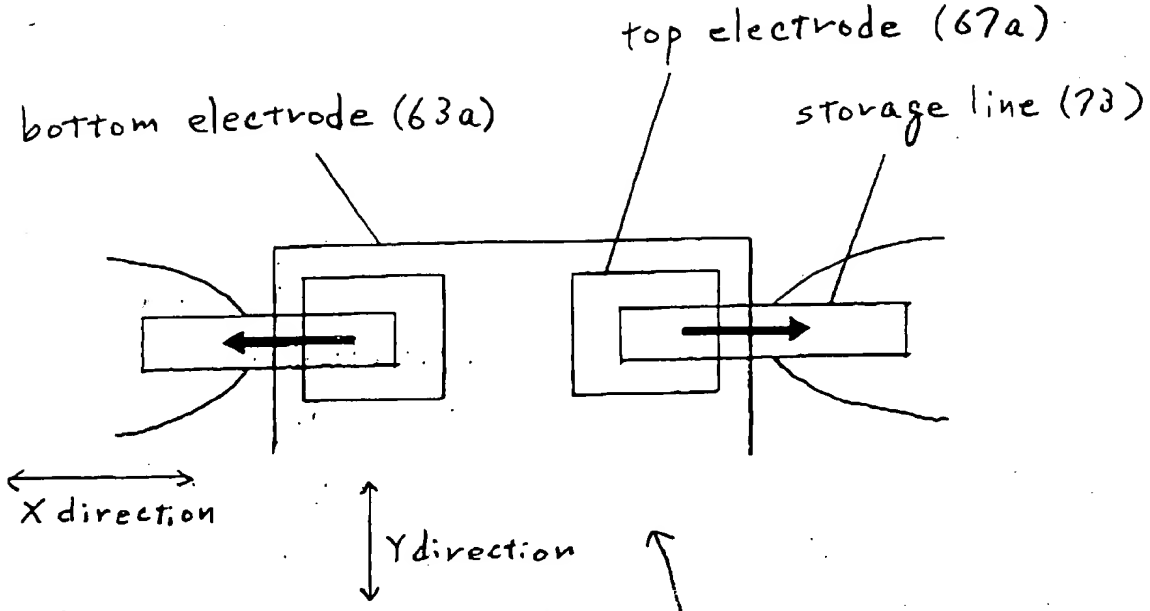
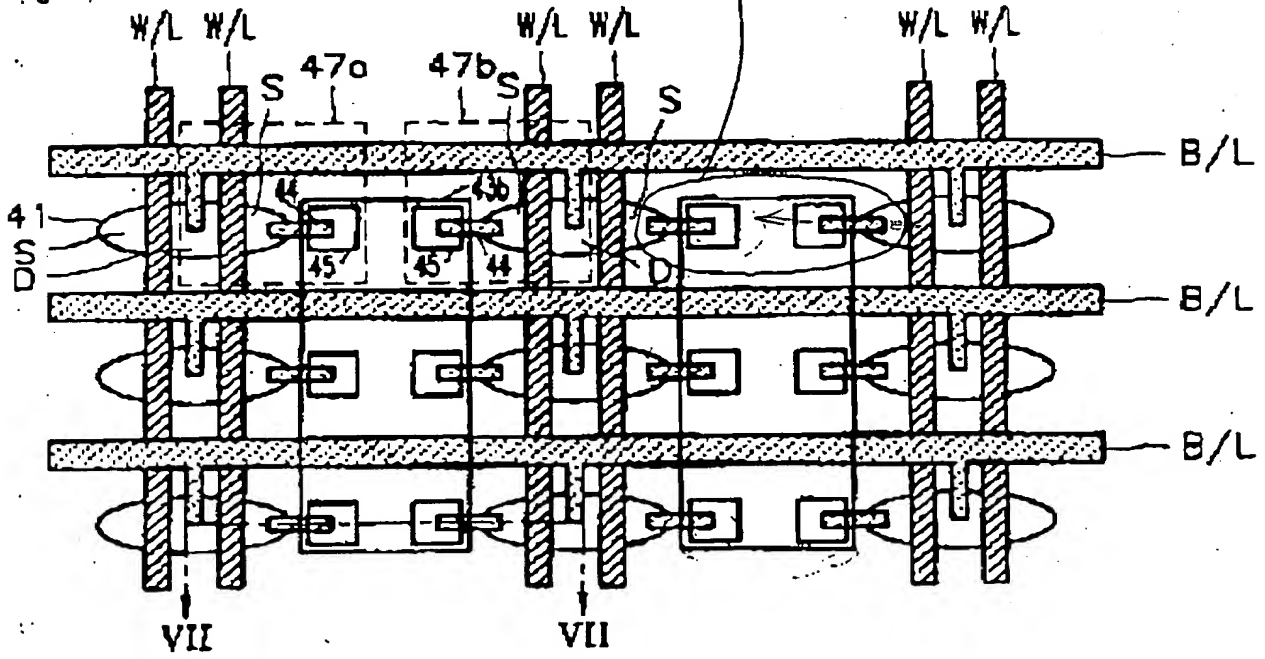


Fig. 6



ATTACHMENT
FIG. 6 OF CHIN